**IN THE CLAIMS:**

1. (Currently Amended) A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

a trench located adjacent a side of the channel region;

an isolation structure located in the trench;

a sidewall spacer located over at least one sidewall of the trench distal the channel region, wherein an interface exists between the sidewall spacer and the isolation structure; and

a source/drain region located over the isolation structure.

2. (Original) The semiconductor device as recited in Claim 1 wherein the trench is a first trench and the semiconductor device further includes a second trench located on an opposing side of the channel region, wherein the isolation structure is a first isolation structure located in the first trench and the semiconductor device further includes a second isolation structure located in the second trench, and wherein the source/drain region is a first source/drain region and the semiconductor device further includes a second source/drain region located over the second isolation structure.

3. (Original) The semiconductor device as recited in Claim 1 wherein the source/drain region comprises polysilicon.

4. (Original) The semiconductor devices as recited in Claim 1 wherein the source/drain region comprises epitaxial silicon.

5. (Previously Presented) The semiconductor device as recited in Claim 1 wherein an oxide layer is located between the sidewall spacer and the at least one sidewall of the trench.

6. (Previously Presented) The semiconductor device as recited in Claim 1 wherein the sidewall spacer comprises a nitrided layer.

7. (Original) The semiconductor device as recited in Claim 1 wherein the isolation structure comprises an oxide.

8. (Original) The semiconductor device as recited in Claim 1 wherein the source/drain region includes a lightly doped source/drain region having a dopant concentration ranging from about 1E16 atoms/$cm^3$ to about 1E17 atoms/$cm^3$, and a source/drain contact region having a dopant concentration up to about 1E22 atoms/$cm^3$.

9. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

forming a channel region in a semiconductor substrate;

forming a trench adjacent a side of the channel region;

forming an isolation structure in the trench;

forming a sidewall spacer over at least one sidewall of the trench distal the channel region, wherein an interface exists between the sidewall spacer and the isolation structure; and

forming a source/drain region over the isolation structure.

10. (Original) The method as recited in Claim 9 wherein forming the trench includes forming a first trench and the method further includes forming a second trench on an opposing side of the channel region, wherein forming the isolation structure includes forming a first isolation structure in the first trench and the method further includes forming a second isolation structure in the second trench, and wherein forming the source/drain region includes forming a first source/drain region and the method further includes forming a second source/drain region over the second isolation structure.

11. (Original) The method as recited in Claim 9 wherein forming the source/drain region includes forming a polysilicon source/drain region.

12. (Original) The methods as recited in Claim 9 wherein forming the source/drain region includes epitaxially growing the source/drain region from the channel region.

13. (Previously Presented) The method as recited in Claim 9 further including forming an oxide layer between the sidewall spacer and the at least one sidewall of the trench.

14. (Previously Presented) The method as recited in Claim wherein forming a sidewall spacer includes forming a nitrided layer.

15. (Original) The method as recited in Claim 9 wherein forming an isolation structure includes forming an isolation structure comprising an oxide.

16. (Original) The method as recited in Claim 9 wherein forming a source/drain region includes forming a lightly doped source/drain region having a dopant concentration ranging from about 1E16 atoms/$cm^3$ to about 1E17 atoms/$cm^3$, and forming a source/drain contact region having a dopant concentration up to about 1E22 atoms/$cm^3$.

17. (Currently Amended) An integrated circuit, comprising:

semiconductor devices, including;

a channel region located in a semiconductor substrate;

a trench located adjacent a side of the channel region;

an isolation structure located in the trench;

a sidewall spacer located over at least one sidewall of the trench distal the channel region, wherein an interface exists between the sidewall spacer and the isolation structure; and

a source/drain region located over the isolation structure; and

dielectric layers located over the semiconductor devices and having interconnect structures located therein that electrically connect the semiconductor devices to form an operative-integrated circuit.

18. (Original) The integrated circuit as recited in Claim 17 wherein the trench is a first trench and the semiconductor device further includes a second trench located on an opposing side of the channel region, wherein the isolation structure is a first isolation structure located in the first trench and the semiconductor device further includes a second isolation structure located in the second trench, and wherein the source/drain region is a first source/drain region and the

semiconductor device further includes a second source/drain region located over the second isolation structure.

19. (Original) The integrated circuit as recited in Claim 17 wherein the isolation structure comprises an oxide.

20. (Original) The integrated circuit as recited in Claim 17 wherein the semiconductor devices form part of an N-type metal oxide semiconductor (NMOS) device, a P-type metal oxide semiconductor (PMOS) device, a complementary metal oxide semiconductor (CMOS) device, a bipolar device, or a memory device.

21. (Previously Presented) The semiconductor device as recited in Claim 1 wherein the sidewall spacer is not contiguous the side of the channel region.

22. (Previously Presented) The method as recited in Claim 9 wherein the sidewall spacer is not formed contiguous the side of the channel region.